# CLAIMS

1. A method for testing an integrated circuit, comprising:

providing a wafer having multiple die that are separated by a singulation area;

providing a visual functional indicator for each of some or all of the multiple die;

providing test circuitry for each of the some or all of the multiple die that have a visual functional indicator;

powering up the wafer to electrically activate the multiple die and initiate operation of the test circuitry;

performing predetermined tests with the test circuitry for the some or all of the multiple die;

outputting a test result to the visual functional indicator for the some or all of the multiple die; and

using the test result to create a visual indication on the wafer with each visual functional indicator corresponding to the test result.

2. The method of claim 1 further comprising:

physically locating the visual functional indicator within each of some or all of the multiple die.

3. The method of claim 1 further comprising:

physically locating the visual functional indicator external to the some or all of the multiple die and within a scribe area of the wafer.

4. The method of claim 1 further comprising:

implementing the visual functional indicator as a light emitting diode (LED).

5. The method of claim 1 further comprising:

repeating the predetermined tests to test the some or all of the multiple die under a plurality of differing operating conditions to determine whether the some or all of the multiple die are functional within a range of operating conditions.

6. The method of claim 1 further comprising:

providing multiple visual indicators on each of the some or all of the die, each of the multiple visual indicators indicating functional operation of a separate predetermined portion of a predetermined one of the some or all of the multiple die.

7. The method of claim 1 further comprising:

implementing the visual functional indicator as a binary coded decimal (BCD) light emitting diode (LED) that asserts a predetermined decimal upon passing a corresponding predetermined functional test.

8. The method of claim 1 further comprising:

singulating the multiple die and segregating functional die of the multiple die from non-functional die of the multiple die based upon the visual indication.

9. The method of claim 1 further comprising:

recording the visual indication with either a camera or a high resolution imager to form a data base that is used by a singulation tool to singulate the multiple die and segregate the multiple die based on the visual indication.

10. An integrated circuit comprising:

at least one module for providing a predetermined function during a normal operating mode;

a test circuit coupled to the at least one module, the test circuit selectively testing the at least one module by providing a predetermined input test signal and receiving a result signal in response thereto;

a visual indicator coupled to the test circuit, the visual indicator providing an indication from testing of the at least one module.

11. The integrated circuit of claim 10 further comprising:

a plurality of modules and a plurality of multiple visual indicators, each of the plurality of visual indicators corresponding to a

test result of a predetermined one of the plurality of modules.

12. The integrated circuit of claim 10 wherein the visual indicator is used by both the at least one module and the test circuit respectively during a normal operating condition and during a test operating condition.

13. An integrated circuit comprising:

at least one module for providing a predetermined function during a normal operating mode;

a test circuit coupled to the at least one module, the test circuit selectively testing the at least one module by providing a predetermined input test signal and receiving a result signal in response thereto; and

an integrated circuit pin coupled to the test circuit, the integrated circuit pin receiving a test indication signal from the test indication signal in response to the result signal.

14. The integrated circuit of claim 13 wherein an external visual indicator coupled to the test circuit at the integrated circuit pin, the visual indicator providing an indication from testing of the at least one module.

15. A semiconductor wafer, comprising:

a plurality of die separated by a region to be subsequently scribed;

test circuitry contained within the plurality of die; and

a plurality of visual indicators, each of the plurality of visual indicators coupled to the test circuitry of a predetermined different one of the plurality of die, the plurality of visual indicators indicating which die passed a functional test implemented by the test circuitry.

16. The semiconductor wafer of claim 15 wherein the plurality of visual indicators is positioned within the region to be subsequently scribed.

17. The semiconductor wafer of claim 15 wherein the plurality of visual indicators is positioned within each of the plurality of die.

18. The semiconductor wafer of claim 15 wherein each of the plurality of visual indicators is a light emitting diode (LEDs).

19. The semiconductor wafer of claim 15 wherein a portion of the plurality of visual indicators is used for both a test mode of operation and a normal functional mode of operation.